WHAT IS CLAIMED IS:

1. A semiconductor memory device accommodated in a package, comprising:

a reference voltage generating circuit generating a reference voltage based on an external power supply voltage;

a voltage dividing circuit dividing an external voltage supplied from the outside of said package into a plurality of divided voltages having voltage values different from each other;

a select circuit selecting one standard voltage from among said reference voltage and said plurality of divided voltages in accordance with a control signal supplied from the outside of said package; and

an internal voltage generating circuit generating an internal power supply voltage based on said standard voltage.

2. The semiconductor memory device according to claim 1, wherein said voltage dividing circuit includes

an external power supply node provided with said external power supply voltage as said external voltage, and

a plurality of resistance elements connected in series between said external power supply node and a ground node, and dividing said external power supply voltage into a plurality of divided voltages having voltages values different from each other.

3. The semiconductor memory device according to claim 1, wherein said voltage dividing circuit includes

a data mask pin provided with a data mask signal voltage as said external voltage, and

a plurality of resistance elements connected in series between said data mask pin and a ground node, and dividing said data mask signal voltage into a plurality of divided voltages having voltage values different from each other.

4. The semiconductor memory device according to claim 1, wherein said select circuit includes

a divided voltage select portion selecting one selected voltage from among said plurality of divided voltages in accordance with a plurality of select signals provided corresponding to said plurality of divided voltages, and

a standard voltage select portion selecting said reference voltage as said standard voltage when a test mode control signal takes one logical level, and selecting said selected voltage as said standard voltage when said test mode control signal takes another logical level.